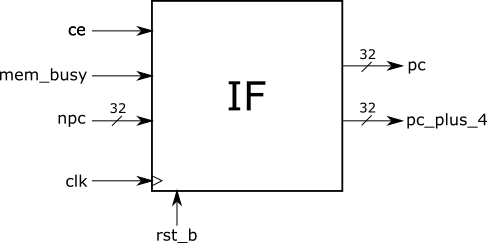
RISC-V IF

**RISC-V Instruction Fetch Module**



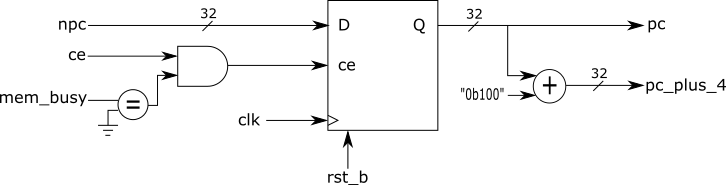
# Description

This is the RISC-V Processor’s instruction fetch module. It tracks the processors program counter and returns the current program counter value alongside the next sequential program counter value. The current program counter value is always passed to instruction memory to fetch the current instruction to be processed. The program counter will store the value presented on “npc” on the rising edge of every clock cycle if “ce” is asserted and “mem\_busy” is de-asserted.

# Data Dictionary

|  |  |
| --- | --- |
| **Signal Name** | **Description** |
| clk | System clock signal |
| rst\_b | System reset signal |
| npc | The next value for the program counter |
| ce | Chip enable signal |
| mem\_busy | Memory is currently busy, halt system |
| pc | The current value of the program counter |
| pc\_plus\_4 | The next sequential program counter value |

# Implementation



If “ce” enable is asserted and “mem\_busy” is de-asserted, the chip enable for the 32x1-bit D-Flip flops is asserted, allowing “npc” to propagate to “pc” on the next rising edge of the clock. When “rst\_b” is de-asserted the D-Flip Flop’s output is forced to 0. The current output of the D-Flip flop has 4 or “100” in binary added to it, to produce the next sequential location.

# Revision History

* Revision 0.01 – Initial Revision, created document with block diagram, module description and data dictionary
* Revision 0.02 – Updated documentation to encompass changes made to core to marry with the SCC